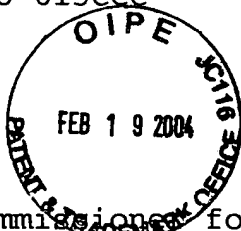
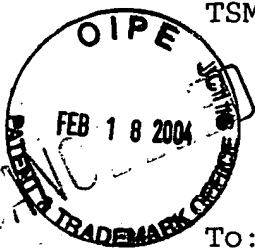


TSMC-98-615CCC



February 9, 2004

To: Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572  
28 Davis Avenue  
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/733,722 12/11/03

S.L. Shue et al.

IMPROVED SIDEWALL COVERAGE FOR  
COPPER DAMASCENE FILLING

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

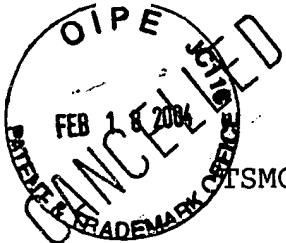
The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
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P.O. Box 1450, Alexandria, VA 22313-1450, on February 7, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date SB Ackerman 2/17/04



TSMC-98-615CCC

U.S. Patent 5,316,974 to Crank, "Integrated Circuit Copper Metallization Process using a Lift-Off Seed Layer and a Thick-Plated Conductor Layer", teaches limiting the seed layer to the bottom of the trench so that the filler plug grows (by electroplating) from the bottom up and not from the vertical sides, thereby avoiding void formation.

U.S. Patent 5,674,787 to Zhao et al., "Selective Electroless Copper Deposited Interconnect Plugs for ULSI Applications", discloses a method for utilizing electroless copper deposition to selectively form encapsulated copper plugs to conductive regions on a semiconductor.

U.S. Patent 5,677,244 to Venkatraman, "Method of Alloying an Interconnect Structure with Copper", discloses doping aluminum with copper by first laying down an agglomerated copper film, then depositing the aluminum copper then heating so as to diffuse the copper islands throughout the aluminum.

U.S. Patent 5,814,557 to Venkatraman et al., "Method of Forming an Interconnect Structure", describes a process for filling the trench/hole of a damascene structure by depositing two different conductors one after the other.

Sincerely,

Stephen B. Ackerman, Reg. #37761

